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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,596	09/12/2001	Anton Gunzinger	FREI P033US-2	8857

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EXAMINER

ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
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2183

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114

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/954,596

Applicant(s)

Gunzinger, Anton

Examiner

Richard Ellis

Group Art Unit

2183

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

- ☒ Responsive to communication(s) filed on March 8, 2003.
- ☐ This action is FINAL
- ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- ☒ Claim(s) 16-31 is/are pending in the application.
- ☐ Of the above claim(s) is/are withdrawn from consideration.
- ☐ Claim(s) is/are allowed.
- ☒ Claim(s) 16-31 is/are rejected.
- ☐ Claim(s) is/are objected to.
- ☐ Claim(s) are subject to restriction or election requirement.

Application Papers

- ☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
- ☐ The proposed drawing correction, filed on is ☐ approved ☐ disapproved.
- ☐ The drawing(s) filed on is/are objected to by the Examiner.
- ☐ The specification is objected to by the Examiner.
- ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

- ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
 - ☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been received
 - ☐ received in Application No. (Series Code/Serial Number)
 - ☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received:

Attachment(s)

- ☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)
- ☐ Interview Summary, PTO-413
- ☐ Notice of References Cited, PTO-892
- ☐ Notice of Informal Patent Application, PTO-152
- ☐ Notice of Draftsperson's Patent drawing Review, PTO-948
- ☐ Other

Office Action Summary

1. Claims 16-31 are presented for examination.
2. Applicant's amendment of March 8, 2003 has been entered into the application.
3. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16-31 are rejected under 35 USC 102(b) as being clearly anticipated by Parrish et al., U.S. Patent 5,117,350.

Parrish et al. was cited as a prior art reference in applicant's information disclosure statement, paper number 3, received January 8, 2002.

Parrish et al. taught (e.g. see figs. 1-14) the invention as claimed (as per claim 16), including a data processing ("DP") system comprising:

- A) a method of operating a parallel computer system (fig. 2) having at least first and second processor elements (100, 120), each processor element comprising a processor (col. 14 lines 10-11) a local program memory (col. 14 lines 11-12), a local data memory (col. 14 lines 11-12), a communications manager (fig. 8b-8d, 419, 439, 459), and an operating system (col. 15 lines 30-31) within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus (fig. 2, 115, 116, 135, 136, fig. 8b-8d, 401, 421, 441); the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network (fig. 2, 160, fig. 8b-8d, 460); the processor elements each executing an application (col. 13 lines 35-36); each communications manager further containing a plurality of predefined values (fig. 8b-8d, 419, containing six predefined values, 439, containing four predefined values, 459, containing five predefined values) each of which, in the event of a match of one of the predetermined values to a global address in a message causes storage of results of an associated computation in local data memory (col. 13 lines 49-68); the method comprising the steps of;
- B) writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications

manager of the first processor element (col. 13 lines 49-54);

- C) adding, by the communications manager, a global address to the result of the computation (col. 13 lines 54-58);
- D) propagating, on the message-passing communications network (460), a message comprising the global address and the result of the computation (col. 13 lines 58-60);
- E) receiving the message, via the message-passing communications network (460), by the communications manager of the second processor element (col. 13 lines 58-60);
- F) comparing, by the communications manager of the second processor element, the global address in the message with the plurality of predefined values for a match (col. 13 lines 60-62); and,
- G) in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory (col. 13 lines 62-68).

5. As to claim 17, Parrish et al. taught that the predefined values were further characterized as comprising an address window (fig. 8, DCM1, DCM2, SGM1, RGM1), each window comprising an initial address (e.g., DCM1 of Node A begins at address 512K) and an end address (e.g., DCM1 of Node A ends at address 768K), a match comprising the global address falling between the initial address and the end address (col. 13 lines 49-52).

6. As to claim 18, Parrish et al. taught that computing a local address comprised adding an offset of one or more bits to the global address, yielding the local address (col. 13 lines 60-68).

7. As to claim 19, Parrish et al. taught computing a local address comprised replacing more or more bits of the global address by a base value, yielding the local address (col. 13 lines 60-68).

8. As to claim 20, taught that the propagating step comprised propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements (fig. 8b-8d, DCM2 is allocated in two (Node A and Node C) out of three of the exemplarily nodes).

9. As to claim 30, Parrish et al. taught that the predefined values were further characterized as comprising at least two address windows (fig. 8b-8d, DCM1, DCM2, SGM1


all present in Node A), each window comprising an initial address (DCM1 512K, DCM2, 768K, and SGM1 2048K) and an end address (DCM1 768K, DCM2 1280K, and SGM1 2304K), a match comprising the global address falling between the initial address and the end address of at least one of the at least two address windows (col. 13 lines 49-68).

10. As to claims 21-25 and 31, they do not teach or define above the invention claimed in claims 16-20 and 30 and are therefore rejected under Parrish et al. for the same reasons set forth in the rejection of claims 16-20 and 30, supra. As to claim 21's additional limitation of the local data memories of the first and second processing unit not on a common bus, as it clearly seen from figs. 8b-8d, the local memories of each node are not connected to a common bus, but instead to separate busses (401, 421, 441).
11. As to claims 26-29, they do not teach or define above the invention claimed in claims 16-25 and 30-31 because claim 26 is identical to claim 16 plus claim 17, claim 27 is identical to claim 16 plus claim 20, claim 28 is identical to claim 21 plus 22, and claim 29 is identical to claim 21 plus 25 and they are therefore rejected under Parrish et al. for the same reasons set forth in the rejection of claims 16-25 and 30-31, supra.
12. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.
13. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).
14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
March 26, 2003


Richard Ellis
Primary Examiner
Art Unit 2183